REMARKS

Claims 1-4 and 6-32 are pending in the application.

Claims 2-4, 6, 9, 11, 12, 14-20, 22-30 are original.

Claims 31-32 are new.

Claims 1, 7, 8, 10, 13, 21, and 27 are currently amended.

Claim 5 is cancelled.

Claims Rejections – 35 USC § 112

Claims 1-7, 10-11, 13 and 21-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subjected matter which applicant regards as the invention.

Claim 1 is currently amended, as suggested, to recite a comparator to determine failure of the memory cells to store the data, by comparing the stored data with expected data. Support for this amendment is, among other places, in the specification on page 3, lines 2-3. No new matter is added. Claim 1 is now in condition for allowance.

Claims 4 and 5 previously contained the same limitations, as noted. Claim 5 is now canceled. Claim 4 remains in condition for allowance.

Claim 7 is currently amended, as suggested, by adding a comma and the word "data" before the word "bits". Claim 7 is now in condition for allowance.

Claim 10 is currently amended to recite "the fail bit detecting circuit receives data bits sent via the column select circuit in synchronization with read-out enable signals". No new matter is added. Claim 10 is now in condition for allowance.

Claim11 is rejected under 35 U.S.C. 112, second paragraph. The applicant respectfully traverses this rejection.

Claim 11 is supported, for example, in Figure 10 (see steps S300 and S310), and page 7, line 33, and page 11, lines 10-19. Initialization of the fail bit counter and the latch circuit occurs in step S310 of Figure 10 after receiving a fail bit detection command (step S300, Figure 10) at the beginning of the fail bit counting test process. It is typical to initialize components in the *beginning* of a process. For at least this reason Claim 11 is in condition for allowance.

Claim 13 is currently amended to eliminate the lack of antecedent basis problem. Claim 13 is now in condition for allowance.

Claim 21 is currently amended to recite the step of registering failure occasions in which the inputted expected data does not correspond with the stored test data. The following elements of claim 21 are deleted; "the compared outputted expected data", and "a register", thus removing all grounds for rejection. Therefore claim 21 is now in condition for allowance.

Claim 27 is currently amended to recite the separate step of incrementing the column address, as suggested. No new matter is added.

Claims 27 is rejected under 35 U.S.C. 112, second paragraph. The applicant respectfully traverses this rejection.

Claim 27 recites storing a fail code determined according to the counted number. Support for determining the fail code is on page 12, lines 23-33, and page 13, lines 1-9. The fail code represents the counted number of fail bits. The fail code is a hexadecimal code converted from the binary counted number of fail bits (page 12, line 27, page 13, lines 1 and 8). The fail code may be further utilized in an algorithm, for example an error code algorithm (page 13, line 14, for example), and hexadecimal encoding is a useful format. For at least this reason Claim 27 is in condition for allowance.

Claims 2-3, 6, 22-26, and 28-30 are rejected under 35 U.S.C. 112, second paragraph because they respectively depend on claims 1, 21, and 27. The applicant asserts that claims 2-3, 6, 22-26, and 28-30, which recite additional novel and non-obvious features of their respective base claim, are also in condition for allowance.

Claims Rejections – 35 USC § 103

Claims 1-18 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raad et al. (6,243,840 and Raad hereinafter) in view of Hill et al. (6,141, 779 and Hill hereinafter). The applicants respectfully traverse this rejection.

Claim 1 is currently amended to recite a comparator to determine failure of the memory cells to store the data, by comparing the stored data with expected data. Support for this amendment is on page 3, lines 2-3, page 11, lines 27-30, and Figures 1, 3, and 10. No new matter is added. The comparator determines failure based on the memory cells ability to store data accurately. Speed and timing, in which a clock signal is needed, are not necessary elements in claim 1.The comparator determines failure only by comparing stored data with expected data. In other words, a failure would not be determined by any timing issue.

In stark contrast, Raad teaches a semiconductor memory device that is operated in a *speed* test mode (Abstract, line 1-20). Raad does not teach comparing data contents without

needing to consider timing issues In particular, when the control circuit 12 is instructed to operate the memory device 10 in the speed test mode, the control circuit provides a speed-test-enable signal STE that enables the test mode circuit 36 to perform speed testing of the memory device. The test mode circuit 36 also receives the system clock signal CLK, and provides a comparison or pass/fail signal to the data output register 28 (column 4, lines 52-59, emphasis added). The comparator 38 receives the signal STE from the control circuit 12 (figure 1) that enables the comparator to compare data on the internal data output bus 37 to the data pattern provided by the data background circuit 40 at a time referenced to the system clock signal CLK (column 5, line 66 – column 6, line 4, emphasis added). A pass/fail condition is established based on if the read-accessed data is available on the internal bus 37 at the referenced time (column 6, lines 10-13, emphasis added). The assumption is made, for the success of this speed test, that no cell defect or other functional errors have occurred, and that access time is the only variable at issue (column 6, lines 15-17, emphasis added). This assumption precludes testing the type of memory cell testing of claim 1, and teaches away from simply comparing data contents without needing to consider timing issues. Therefore claim 1 is not obvious in reading Raad in view of Hill, and claim 1 is allowable.

Claims 2-4, and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raad et al., as applied to claim 1, and Hill et al. The applicant asserts that claims 2-4, and 6-7, which recite additional novel and non-obvious features of their base claim, are also in condition for allowance.

Claim 5 is canceled.

Claim 8 is currently amended to recite determining failure of the memory cells to store the data, by comparing the selected data bits with the expected data bits. Support for this amendment is on page 3, lines 2-3, page 11, lines 27-30, and Figures 1, 3, and 10. No new matter is added. The same arguments asserted for claim 1 above apply to currently amended claim 8. Claim 8 determines failure of the memory cells to store the data accurately (so the stored data compares with the expected data), but Raad only teaches failure based on timing. Therefore claim 1 is not obvious in reading Raad in view of Hill, and claim 1 is allowable.

Claims 9-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raad et al., as applied to claim 8, and Hill et al. The applicant asserts that claims 9-20, which recite additional novel and non-obvious features of their base claim, are also in condition for allowance.

Claim 21 is currently amended to recite comparing the stored expected data with the stored test data to determine failure of the memory cells to store data; and registering failure

occasions in which the inputted expected data does not correspond with the stored test data. Support for this amendment is on page 3, lines 2-3, page 11, lines 27-30, and Figures 1, 3, and 10. No new matter is added. The same arguments asserted for claims 1 and 8 above apply to currently amended claim 21. Claim 21 determines failure of the memory cells to store the data accurately (so the stored data compares with the expected data), but Raad only teaches failure based on timing. Therefore claim 1 is not obvious in reading Raad in view of Hill, and claim 1 is allowable.

Claims 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raad et al., as applied to claim 21, and Hill et al. The applicant asserts that claims 22-26, which recite additional novel and non-obvious features of their base claim, are also in condition for allowance.

Claims 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raad et al. (6,243,840 and Raad hereinafter) in view of Hill et al. (6,141,779 and Hill hereinafter) and Beffa et al. (6,032,264 and Beffa hereinafter).

Claim 27 recites determining whether the selected data bits each matches corresponding expected data bits applied from the outside. The same arguments asserted for claims 1, 8, and 21 above apply to currently amended claim 27. Claim 27 determines failure of the memory cells to store the data accurately (so the stored data compares with the expected data), but Raad only teaches failure based on timing. Therefore claim 27 is not obvious in reading Raad in view of Hill and Beffa, and claim 27 is therefore allowable.

Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raad et al., as applied to claim 27, and Hill, and Beffa. The applicant asserts that claims 28-30, which recite additional novel and non-obvious features of their base claim, are also in condition for allowance.

Allowable Subject Matter

Claims 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In keeping with the Examiner's suggestion, new claims 31 and 32 are added.

Claim 31 is in independent form and contains all the limitations of original claim 19, 16 and its base (claim 8).

Claim 32 is in dependent form and contains all the limitations of original claim 20.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-4 and 6-32 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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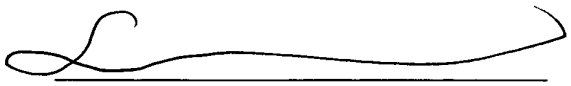

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Limited Under 37 CFR § 10.9(b)

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